Lens Driver IC for Camcorder and Security-Camera Incorporating Iris Control

1 Features

- H-Bridge Motor Driver
- Voltage drive system 256-step microstep drivers
  - 2 systems
  - Super low noise Zoom and Focus driver
- Built-in Iris controller
- Motor control by 4-line serial data communication
- 2 systems of open-drain for driving LED
- PCB space saving
- Low power consumption of Iris drive by PWM
- Small Package and Footprint
  - 44 pin QFN (Without Thermal Pad)
  - 6.00mm x 6.00mm

2 Applications

- Camcorder
- security-camera
- Robot
- Precision industrial equipment

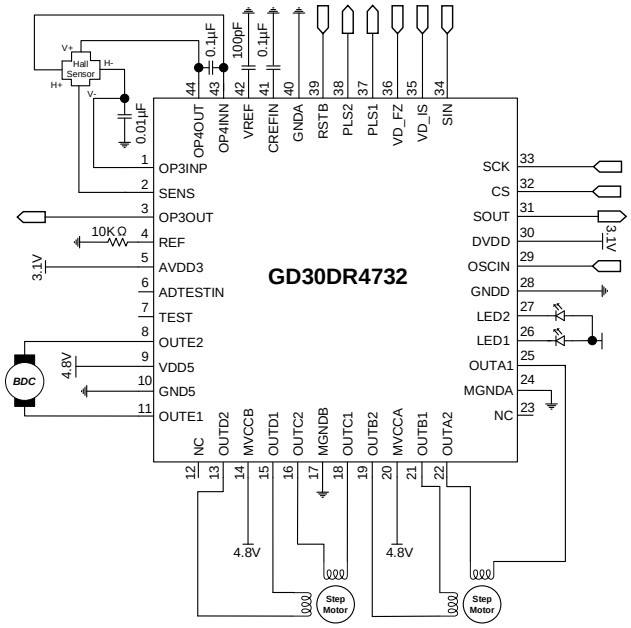
3 Description

The GD30DR4732 is a lens motor driver IC for camcorder and security-camera featuring the functions of Iris control. Voltage drive system and several torque ripple correction techniques enable super-low noise microstep drive.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DR4732	QFN44	6.00 mm × 6.00 mm

1. For packaging details, see *Package Information* section.



Simplified Application Schematic

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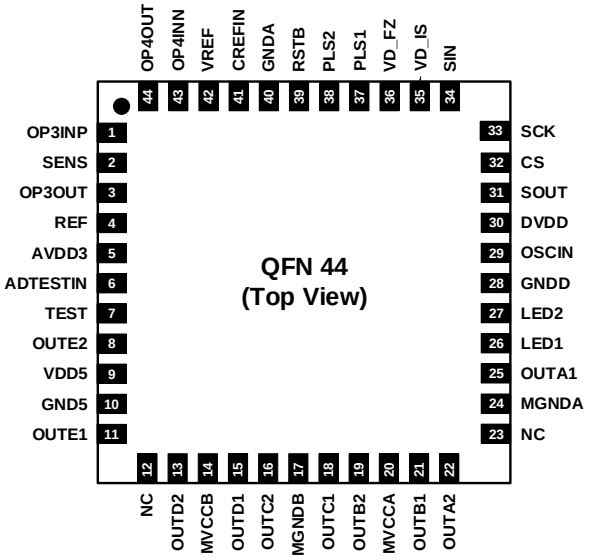
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE[1]	FUNCTION
NAME	DFN44		
OP3INP	1	I	Hall signal amplifier non-inverting input.
SENS	2	O	Hall current bias output.
OP3OUT	3	O	Hall signal amplifier output.
REF	4		Resistor connection for Hall current bias setting.
AVDD3	5	P	3 V analog power supply.
ADTESTIN	6	I	ADC test input.
TEST	7	I	Test mode input.
OUTE2	8	O	Motor output E2.
VDD5	9	P	Power supply for Iris.
GND5	10	G	GND for Iris.
OUTE1	11	O	Motor output E1.
NC	12		NC.
OUTD2	13	O	Motor output D2.
MVCCB	14	P	Power supply for motor B.
OUTD1	15	O	Motor output D1.
OUTC2	16	O	Motor output C2.
MGNDB	17	G	GND for motor B.

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PIN		PIN TYPE[1]	FUNCTION
NAME	DFN44		
OUTC1	18	O	Motor output C1.
OUTB2	19	O	Motor output B2.
MVCCA	20	P	Power supply for motor A.
OUTB1	21	O	Motor output B1.
OUTA2	22	O	Motor output A2.
NC	23		NC.
MGNDA	24	G	GND for motor A.
OUTA1	25	O	Motor output A1.
LED1	26	I	Open-drain 1 for driving LED.
LED2	27	I	Open-drain 2 for driving LED.
GNDD	28	G	Digital GND.
OSCIN	29	I	OSCIN input.
DVDD	30	P	3 V digital power supply.
SOUT	31	O	Serial data output.
CS	32	I	Chip select signal input.
SCK	33	I	Serial clock input.
SIN	34	I	Serial data input.
VD_IS	35	I	Iris video sync. signal input.
VD_FZ	36	I	Focus zoom sync. signal input
PLS1	37	O	Pulse 1 output.
PLS2	38	O	Pulse 2 output.
RSTB	39	I	Reset signal input.
GNDA	40	G	3V analog GND.
CREFIN	41		(AVDD3)/2 capacitor connection pin.
VREF	42	O	Reference voltage for Hall sensor.
OP4INN	43	I	Midpoint bias amplifier inverting input.
OP4OUT	44	O	Midpoint bias amplifier output.

1. I = input, O = output, P = power, G = ground.

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5 Parameter Information

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD3[1]	Controller supply voltage	−0.3		4.0	V
DVDD[1]					
MVCCA[1]	Supply voltage for motor controller 1	−0.3		6.0	V
MVCCB[1]					
VDD5[1]	Supply voltage for motor controller 2	−0.3		6.0	V
Topr[2,4]	Operating ambient temperature	−20		85	°C
Tj[2]	Operating junction temperature	−20		125	°C
Tstg[2]	Storage temperature	−55		125	°C
OUTA1, OUTA2 OUTB1, OUTB2 OUTC1, OUTC2 OUTD1, OUTD2	Motor driver 1 (focus, zoom) H bridge drive current (DC current)	−0.25		+0.25	A/ch
OUTE1, OUTE2	Motor driver 2 (iris) H bridge drive current (DC current)	−0.15		+0.15	A/ch
IM(pulse)	Instantaneous H bridge drive current	−0.4		+0.4	A/ch
OP3INP, OP4INN ADTESTIN REF, CREFIN[3]	Input Voltage Range	−0.3		AVDD3 + 0.3	V
TEST, OSCIN CS, SCK, SIN VD_IS, VD_FZ, RSTB[3]		−0.3		DVDD + 0.3	V
OP3OUT, OP4OUT SENS, VREF[3]	Output Voltage Range	−0.3		AVDD3 + 0.3	V
PLS1, PLS2, SOUT[3]		−0.3		DVDD3 + 0.3	V
LED1, LED2	Output Current Range		30		mA

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

1. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
2. Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.
3. (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.
4. The power dissipation shown is the value at Ta = 85°C for the independent (unmounted) IC package without a heat sink.

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5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
MVCCx, VDD5[1]	Supply voltage range	3.0	4.8	5.5	V
DVDD, AVDD3[1]		2.7	3.1	3.6	V
VOP3INP, VADTESTIN, VOP4INN, VREF, VCREFIN[2]	Input Voltage Range	−0.3		AVDD3 + 0.3	V
VTEST, VOSCIN VCS, VSCK, VSIN VVD_IS, VVD_FZ VRSTB[2]		−0.3		DVDD + 0.3	V
VOP3OUT, VOP4OUT, VSENS VVREF[2]	Output Voltage Range	−0.3		AVDD3 + 0.3	V
VPLS1,VPLS2, VSOUT[2]		−0.3		DVDD + 0.3	V
IOUTE2, IOUTE1[1]	Output Current Range	−0.15		+0.15	A
IOUTD2, IOUTD1 IOUTC2, IOUTC1 IOUTB2, IOUTB1[1]		−0.25		+0.25	A
ILED1, ILED2[1]				30	mA
Ta	Operating ambient temperature	−20		85	°C

1. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
2. (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.

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5.3 Electrical Characteristics

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CIRCUIT, COMMON CIRCUIT						
$I_{omdisable}$	MVCC supply current on reset	No load, no 27 MHz input		0	3.0	uA
$I_{menable}$	MVCC supply current on enable	Output open		0.5	1.5	mA
$I_{cc3reset}$	3V supply current on reset	No 27 MHz input		0	10.0	uA
$I_{cc3enable}$	3V supply current on enable	Output open		7.0	20.0	mA
$I_{cc5reset}$	VDD5 supply current on reset	No 27 MHz input		0	3.0	uA
$I_{cc5enable}$	VDD5 supply current on rnable	Output open		0.3	1.0	mA
$I_{ccstandby}$	Supply current on standby	RSTB = High, output open, 27 MHz input, total current		5.0	10.0	mA
I_{ccps}	Supply current when FZ is enable and Iris is in power save mode	RSTB = High, output open, 27MHz input, FZ = Enable, total current		6.0	12.0	mA
DIGITAL INPUT / OUTPUT						
$V_{in(H)}$	High-level input	RSTB	0.54 x DVDD		DVDD + 0.3	V
$V_{in(L)}$	Low-level input	RSTB	−0.3		0.2 x DVDD	V
$V_{out(H):SDATA}$	SOUT High-level output	[SOUT] 1mA source	DVDD − 0.5			V
$V_{out(L):SDATA}$	SOUT Low-level output	[SOUT] 1mA Sink			0.5	V
$V_{out(H):MUX}$	PLS1 to 2 High-level output		0.9 x VDD			V
$V_{out(L):MUX}$	PLS1 to 2 Low-level output				0.1 x VDD	V
$R_{pullret}$	Input pull-down resistance	RSTB	50	100	200	KΩ
MOTOR DRIVER 1(FOCUS, ZOOM)						
R_{onFZ}	H bridge ON resistance	IM=100mA			2.5	Ω
I_{leakFZ}	H bridge leak current				0.8	uA
MOTOR DRIVER 2(IRIS)						
R_{onIR}	H bridge ON resistance	IM=50mA			5.0	Ω
I_{leakIR}	H bridge leak current				0.8	uA
LED DRIVER						
R_{onLED}	Output ON resistance	I=20mA, 5V cell			8	Ω
I_{leakIR}	Output leak current				0.8	uA

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Electrical Characteristics (Continued)

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OPAMP3 (HALL Sensor Amp. for output amplifier)						
V_{IN}	Input voltage range		0.5 × AVDD3 − 0.5	0.5 × AVDD3	0.5 × AVDD3 + 0.5	V
V_{OF}	Input offset voltage		−15		15	mV
V_{OL}	Output voltage (Low)	ILOAD=-100mA		0.1	0.2	V
V_{OH}	Output voltage (High)	ILOAD=100mA	AVDD3 − 0.2	AVDD3 − 0.1		V
V_{OG}	Gain	Gain Setting value: 0h	19.7	21.9	24.1	V/V
OPAMP4 (HALL Sensor Amp. for eliminating common-mode voltage)						
V_{IN}	Input voltage range		0.5 × AVDD3 - 0.1		0.5 × AVDD3 + 0.1	V
V_{OF}	Input offset voltage		-10		10	mV
V_{OL}	Output voltage (Low)	ILOAD=-10mA		0.1	0.2	V
V_{OH}	Output voltage (High)	ILOAD=3mA	AVDD3 - 0.5	AVDD3 - 0.2		V
Reference voltage output block						
V_{REF}	Output voltage 1	ILOAD=0, CVREF=100pF	0.5× AVDD3 − 0.1	0.5× AVDD3	0.5× AVDD3 + 0.1	V
V_{REFL}	Output voltage 2	ILOAD=±100mA, CVREF=100pF	V_{REF} − 0.1	V_{REF}	V_{REF} + 0.1	V
Hall bias controller (SENS pin output)						
I_{BL}	Min. output current	REF=10KΩ, SENS=0.7V Setting value: 00 h		0	0.10	mA
I_{B40H}	Output current accuracy 1	REF=10KΩ, SENS=0.7V Setting value: 40 h	0.90	1.02	1.14	mA
I_{BBFH}	Output current accuracy 2	REF=10KΩ, SENS=0.7V Setting value: BE h	2.66	3.02	3.38	mA
SERIAL PORT INPUT[1]						
Sclock	Serial clock		1		5	MHz
T1	SCK low time		100			ns
T2	SCK high time		100			ns
T3	CS setup time		60			ns
T4	CS hold time		60			ns
T5	CS disable high time		100			ns

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Electrical Characteristics (Continued)

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T6	SIN setup time		50			ns
T7	SIN hold time		50			ns
T8	SOUT delay time				60	ns
T9	SOUT hold time		60			ns
T10	SOUT Enable-Hi-Z time				60	ns
T11	SOUT Hi-Z-Enable time				60	ns
T_{SC}	SOUT C load				40	pF
DIGITAL INPUT/OUTPUT[1]						
V_{INH}	High-level input threshold voltage	SCK, SIN, CS,OSCIN, VD_IS, VD_FZ, TEST		1.36		V
V_{INL}	Low-level input threshold voltage	SCK, SIN, CS,OSCIN, VD_IS, VD_FZ, TEST		1.02		V
V_{hysin}	Input hysteresis width	SCK, SIN, CS,OSCIN, VD_IS, VD_FZ, TEST		0.34		V
T_{rst}	RSTB signal pulse width		100			us
V_{DW}	Video sync. Signal width		80			us
$T_{(VD-CS)}$	CS signal wait time 1		400			ns
$T_{(CS-DT1)}$	CS signal wait time 2		5			us
PULSE GENERATOR[1]						
$PL1_{wait}$	Pulse start resolution for pulse 1	OSCIN = 27MHz		20.1		us
$PL1_{width}$	Pulse resolution for pulse 1	OSCIN = 27MHz		1.20		us
$PL2_{wait}$	Pulse start resolution for pulse 2	OSCIN = 27MHz		20.1		us
IRIS CONTROL[1]						
$IRIS_{Sample}$	AD sampling frequency	OSCIN = 27MHz		500		KHz
8 bit DAC for HALL OFFSET ADJUSTMENT[1]						
DAOTHof	Adjustment range (High)			AVDD3		V
DAOTLof	Adjustment range (Low)			0		V
10 bit ADC[1]						
V_{inH}	Input Range (High)			AVDD3 − 0.2		V
V_{inL}	Input Range (Low)		0.2			V
DNL10A	DNLE(Differential linearity error)			1.0		LSB
INL10A	INLE (Integral linearity error)			2.0		LSB
THERMAL SHUTDOWN[1]						
T_{tsd}	Thermal shutdown temperature			150		°C

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Electrical Characteristics(Continued)

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{hys}	Thermal shutdown hysteresis			40		°C
SUPPLY VOLTAGE MONITOR CIRCUIT[1]						
V_{rston}	3.3 V Reset operation			2.27		V
V_{rsthys}	3.3 V Reset hysteresis			0.20		V
$V_{rstFZon}$	MVCCx Reset operation			2.20		V
$V_{rstFZhys}$	MVCCx Reset hysteresis			0.20		V
$V_{rstlSon}$	VDD5 Reset operation			2.2		V
$V_{rstlShys}$	VDD5 Reset hysteresis			0.2		V

1. Guaranteed by design.

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6 Functional Description

6.1 Block Diagram

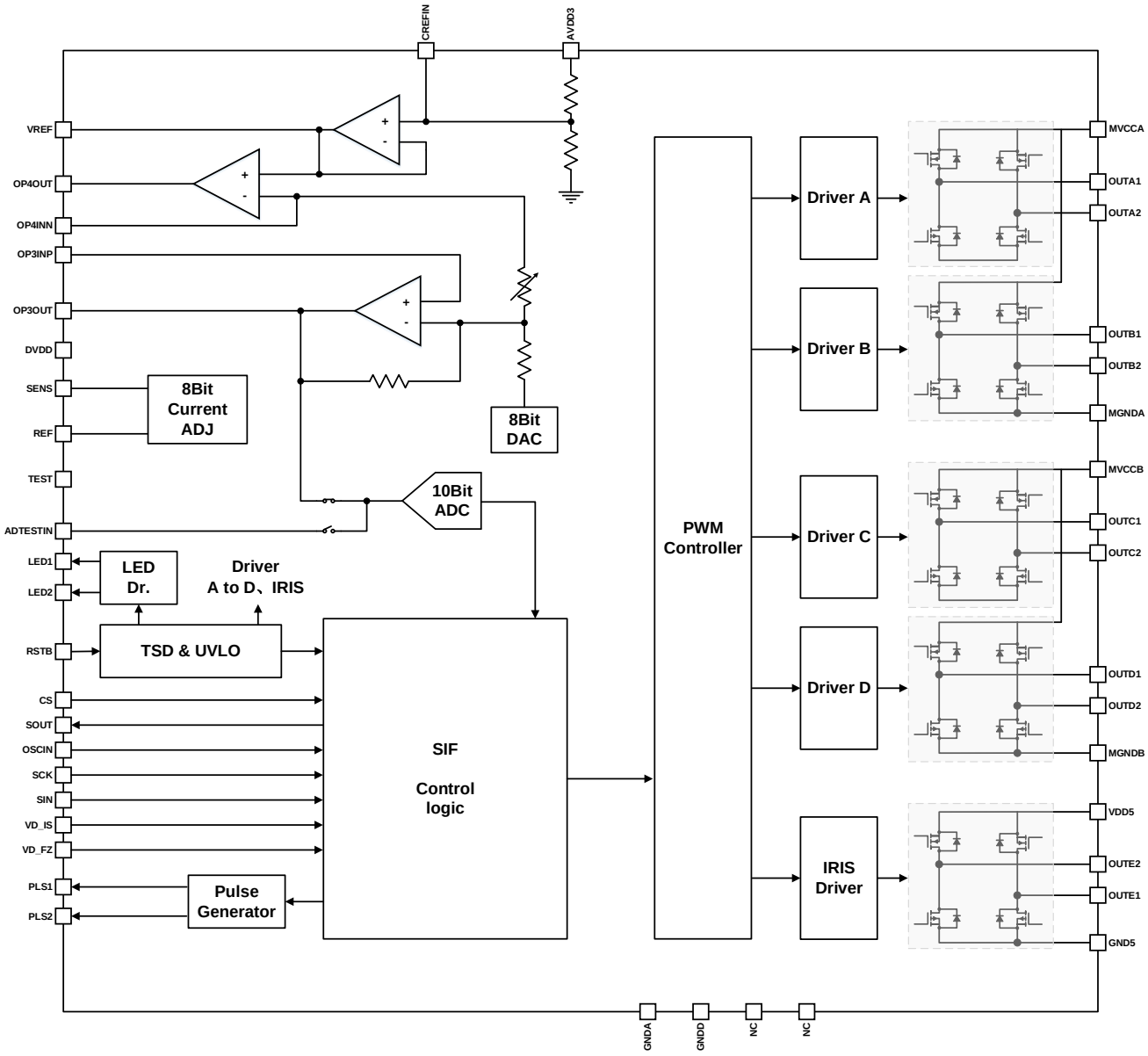

Figure 1. GD30DR4732 Functional Block Diagram[1]

1. This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

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6.2 Serial Interface

6.2.1 Timing Chart

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

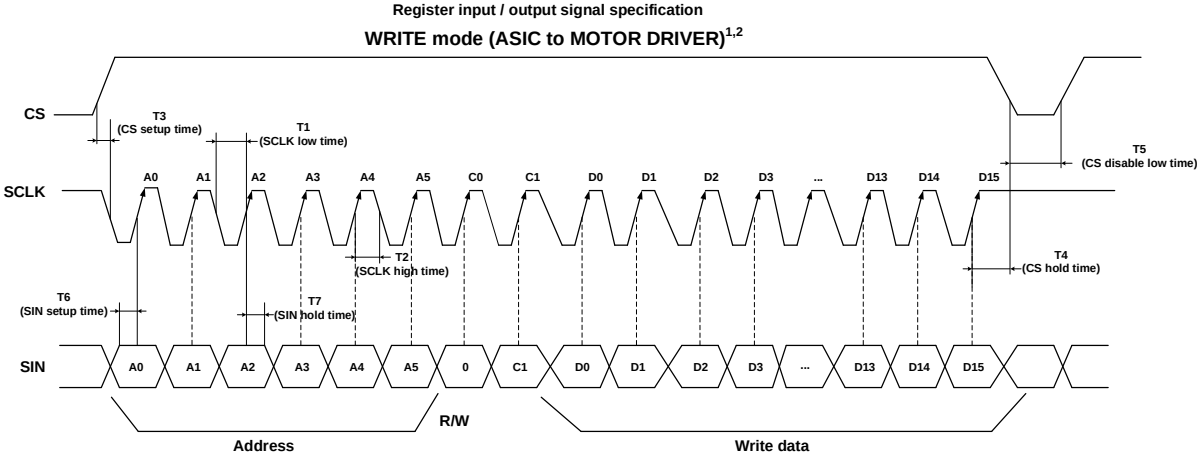

Figure 2. Write Mode Timing

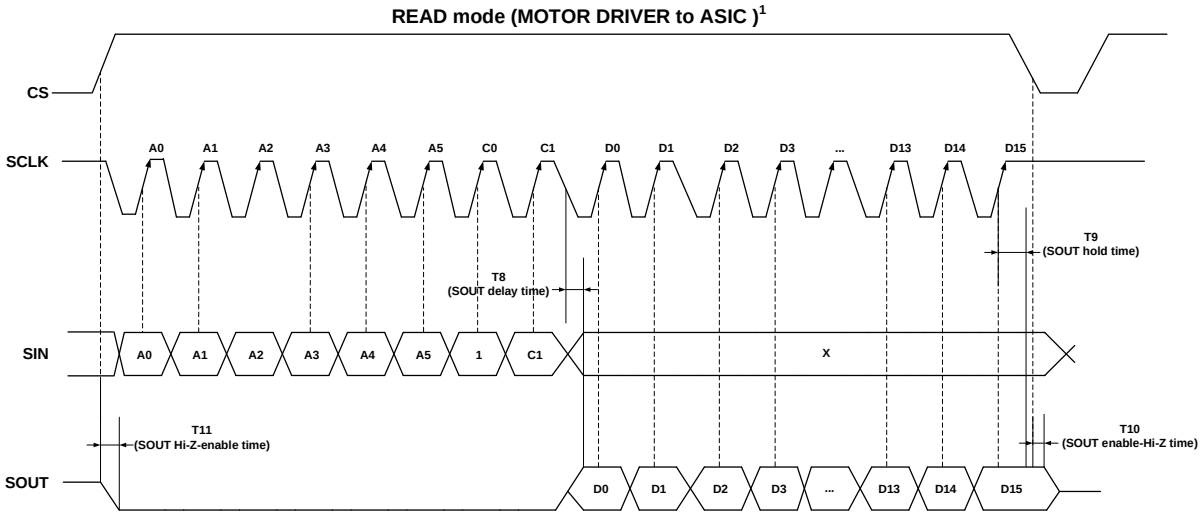

Figure 3. Read Mode Timing

1. CS default value of each cycle (Write / Read mode) starts from Low-level.
2. It is necessary to input the system clock OSCIN at write mode.

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6.2.2 Register Map

Address : 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						IRIS_TGT[9:0]									

Bits	Fields	Descriptions
9:0	IRIS_TGT[9:0]	Iris target

Address : 01h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DGAIN[6:0]							ASOUND_LPF_FC[2:0]			AS_FLT_OFF	DEC_AVE	OVER_LPF_FC_2ND [1:0]		OVER_LPF_FC_1ST [1:0]	

Bits	Fields	Descriptions
15:9	DGAIN[6:0]	PID controller digital gain
8:6	ASOUND_LPF_FC[2:0]	Filter cut-off frequency before PID controller
5	AS_FLT_OFF	Filter before PID controller enable / disable
4	DEC_AVE	Moving average of Iris target
3:2	OVER_LPF_FC_2ND [1:0]	ADC FEEDBACK FILTER (2) CUT-OFF FREQUENCY
1:0	OVER_LPF_FC_1ST [1:0]	ADC FEEDBACK FILTER (1) CUT-OFF FREQUENCY

Address : 02h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_POLE [3:0]				PID_ZERO [3:0]				IRIS_ROUND [3:0]				IRIS_CALC_NR [3:0]			

Bits	Fields	Descriptions
15:12	PID_POLE [3:0]	PID controller pole
11:8	PID_ZERO [3:0]	PID controller zero point
7:4	IRIS_ROUND [3:0]	PID controller differential error cumulative prevention level
3:0	IRIS_CALC_NR [3:0]	PID controller integral error cumulative prevention level

Address : 03h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DT_ADJ_IRIS [1:0]		PWM_IRIS[3:0]			PWM_LPF_FC[2:0]			PWM_FLT_OFF	LMT _ENB	ARW[3:0]			

Bits	Fields	Descriptions
13:12	DT_ADJ_IRIS [1:0]	Dead time correction of Iris block output
11:9	PWM_IRIS[2:0]	PWM frequency of Iris block output
8:6	PWM_LPF_FC[2:0]	LPF cut-off frequency after PID controller
5	PWM_FLT_OFF	LPF after PID controller enable / disable
4	LMT _ENB	PID controller integral stop

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Bits	Fields	Descriptions
3:0	ARW[3:0]	Number of bits in PID controller integrator

Address : 04h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HALL_OFFSET_DAC[7:0]								HALL_BIAS_DAC[7:0]							

Bits	Fields	Descriptions
15:8	HALL_OFFSET_DAC[7:0]	Offset adjustment for hall element output amplifier
7:0	HALL_BIAS_DAC[7:0]	Drive current value for hall element

Address : 05h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			AAF_FC	HALL _ GAIN[3:0]				Reserved		PID_INV	TGT_FL _OFF	TGT_LPF_FC[3:0]			

Bits	Fields	Descriptions
12	AAF_FC	Cut-off frequency of hall element output amplifier
11:8	HALL__GAIN[3:0]	Hall element output amplifier gain
5	PID_INV	PID controller polarity
4	TGT_FL_OFF	Iris target value LPF function enable / disable
3:0	TGT_LPF_FC[3:0]	Iris target value LPF cut-off frequency

Address : 06h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						START1[9:0]									

Bits	Fields	Descriptions
9:0	START1[9:0]	Pulse 1 start time

Address : 07h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1EN	Reserved			WIDTH1[11:0]											

Bits	Fields	Descriptions
15	P1EN	Pulse 1 output enable
11:0	WIDTH1[11:0]	Pulse 1 width

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Address : 08h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						START2[9:0]									

Bits	Fields	Descriptions
9:0	START2[9:0]	Pulse 2 start time

Address : 09h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2EN	Reserved									WIDTH2[5:0]					

Bits	Fields	Descriptions
15	P2EN	Pulse 2 output enable
5:0	WIDTH2[5:0]	Pulse 2 width

Address : 0Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DUTY_ TEST	TGT_IN_TEST[9:0]									

Bits	Fields	Descriptions
10	DUTY_TEST	Iris output duty direct specification enable
9:0	TGT_IN_TEST[9:0]	Iris output duty direct specified value

Address : 0Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_CLIP[3:0]				ADC _TEST	PDWNB	MODESEL _FZ	MODE SEL _IRIS	TESTEN 1	Reserved		ASWMODE[1:0]		Reserved		

Bits	Fields	Descriptions
15:12	PID_CLIP[3:0]	Iris output PWM maximum duty
11	ADC_TEST	ADC read value updated timing
10	PDWNB	Power down of Iris block
9	MODESEL_FZ	VD_FZ polarity selection
8	MODESEL _IRIS	VD_IS polarity selection
7	TESTEN 1	Test mode enable 1
4:3	ASWMODE[1:0]	ADTESTIN pin connection selection

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Address : 0Ch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IRSAD[9:0] (Read Only)							

Bits	Fields	Descriptions
9:0	IRSAD[9:0]	ADC output for Iris (read only)

Address : 0Eh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			AVE_SPEED[4:0]					TGT_UPDATE[7:0]							

Bits	Fields	Descriptions
12:8	AVE_SPEED[4:0]	Iris target moving average speed
7:0	TGT_UPDATE[7:0]	IRS_TGT (iris target) update delay time

Address : 20h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PWMRES[1:0]		PWMMODE[4:0]					DT1[7:0]							

Bits	Fields	Descriptions
14:13	PWMRES[1:0]	Micro step output PWM resolution
12:8	PWMMODE[4:0]	Micro step output PWM frequency
7:0	DT1[7:0]	Start point wait time

Address : 21h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TESTEN2	Reserved			FZTEST[4:0]			

Bits	Fields	Descriptions
7	TESTEN2	Test mode enable 2
4:0	FZTEST[4:0]	PLS1/2 pin output signal selection

Address : 22h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PHMODAB[5:0]						DT2A[7:0]							

Bits	Fields	Descriptions
13:8	PHMODAB[5:0]	α motor phase correction
7:0	DT2A[7:0]	α motor start point excitation wait time

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Address : 23h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPWB[7:0]								PPWA[7:0]							

Bits	Fields	Descriptions
15:8	PPWB[7:0]	Driver B peak pulse width
7:0	PPWA[7:0]	Driver A peak pulse width

Address : 24h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MICROAB[1:0]		LEDB	ENDISAB	BRAKEAB	CCWCWAB	PSUMAB[7:0]							

Bits	Fields	Descriptions
13:12	MICROAB[1:0]	α motor sine wave division number
11	LEDB	LED B output control
10	ENDISAB	α motor enable/disable control
9	BRAKEAB	α motor brake
8	CCWCWAB	α motor rotation direction
7:0	PSUMAB[7:0]	α motor step count number

Address : 25h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTCTAB[15:0]															

Bits	Fields	Descriptions
15:0	INTCTAB[15:0]	α motor step cycle

Address : 27h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PHMODCD[5:0]						DT2B[7:0]							

Bits	Fields	Descriptions
13:8	PHMODCD[5:0]	β motor phase correction
7:0	DT2B[7:0]	β motor start point excitation wait time

Address : 28h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPWD[7:0]								PPWC[7:0]							

Bits	Fields	Descriptions
15:8	PPWD[7:0]	Driver D peak pulse width
7:0	PPWC[7:0]	Driver C peak pulse width

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Address : 29h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MICROCD[1:0]		LEDA	ENDISCD	BRAKECD	CCWCWCD	PSUMCD[7:0]							

Bits	Fields	Descriptions
13:12	MICROCD[1:0]	β motor sine wave division number
11	LEDA	LED A output control
10	ENDISCD	β motor enable/disable control
9	BRAKECD	β motor brake
8	CCWCWCD	β motor rotation direction
7:0	PSUMCD[7:0]	β motor step count number

Address : 2Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTCTCD[15:0]															

Bits	Fields	Descriptions
15:0	INTCTCD[15:0]	β motor step cycle

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6.2.3 Serial Interface Specifications

- Data transfer starts at the rising edge of CS, and stops at the falling edge of CS.
- One unit of data is 24 bits. (24 bits of the following format are called a data set in this book.)
- Address and data are serially input from SIN pin in synchronization with the data clock SCK at CS = 1.
- Data is retrieved at the rising edge of SCK.
- Moreover, data is output from SOUT pin at data readout. (Data is output at the rising edge of SCK.)
- SOUT outputs Hi-Z at CS = 0, and outputs "0" except data readout at CS = 1.
- The control circuit of serial interface is reset at CS = 0.

6.2.4 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

- C0 : Register write / read selection 0 : write mode, 1 : read mode
- C1 : Unused
- A5 to A0 : Address of register
- D15 to D0 : Data written in register

When C0 bit is "0", the write mode is selected. The address and data are retrieved from SIN in synchronization with the rising edge of data clock SCLK, and the data is stored in internal register in synchronization with the rising edge of CS.

SOUT outputs "0" in the write mode.

When the data which is 23 or less bits per 1 processing is received in the write mode, the received data becomes invalid. The data of 25 or more bits is regarded as the continuous write mode, and the write operation is performed whenever the data of 24 bits is received. When the last data set is less than 24 bits in the continuous write mode, it becomes invalid. (The previous data set is valid.)

Even if noise occurs on SCK signal in the continuous write mode and the shifted data is received, pay attention to continue receiving or updating the shifted data.

When C0 bit is "1", the read mode is selected. The address is retrieved from SIN in synchronization with the rising edge of SCK, and then the register value of the address specified is output as LSB first from SOUT, in synchronization with the rising edge of SCK.

When C0 bit is "1", the values of D15 to D0 of SIN do not be cared.

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6.2.5 Formatting

All the SIF functions containing a data register are formatted at RSTB = 0. Characteristic of supply voltage monitor.

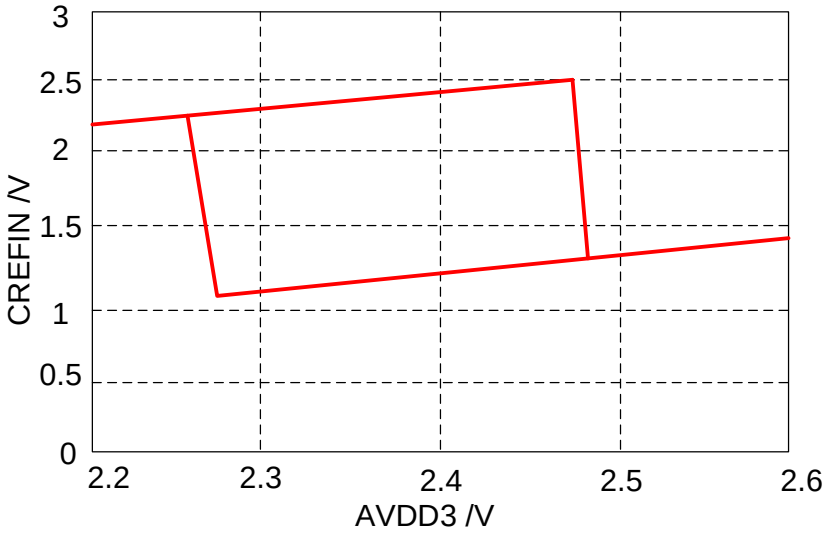

Figure 4. AVDD3 (Operation voltage:2.28V Return voltage: 2.48V)

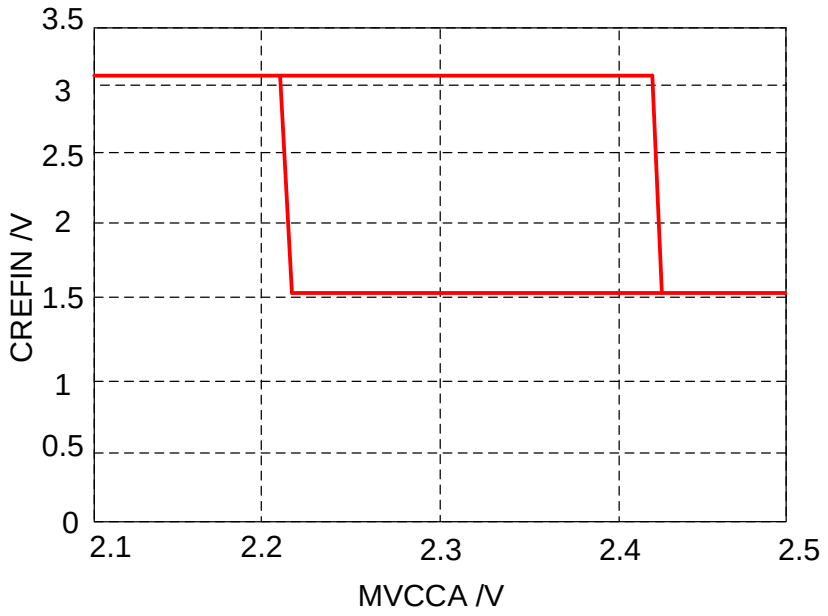

Figure 5. MVCC (Operation voltage:2.22V Return voltage: 2.42V)

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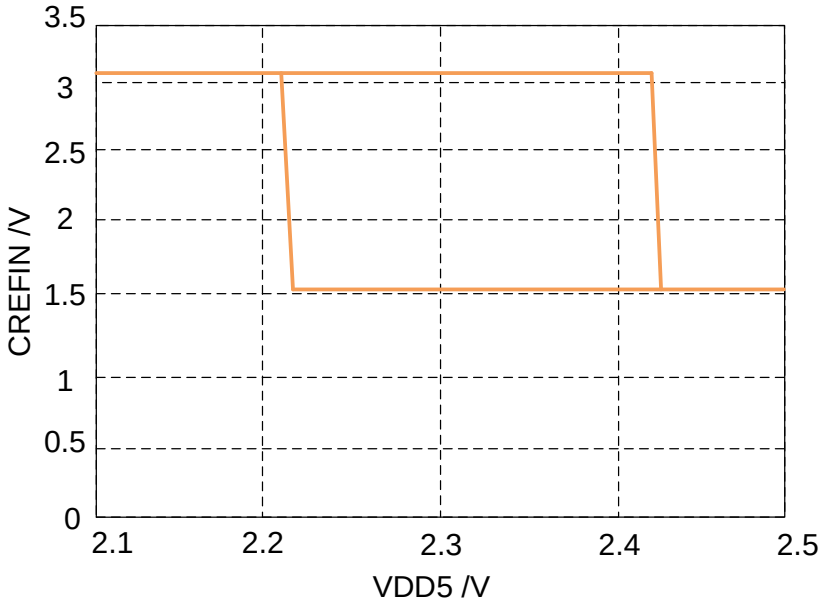

Figure 6. VDD5 (Operation voltage:2.22V Return voltage: 2.42V)

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7 Application

The GD30DR4732 is typically used to drive motors for network and security cameras.

7.1 Typical Application Circuit

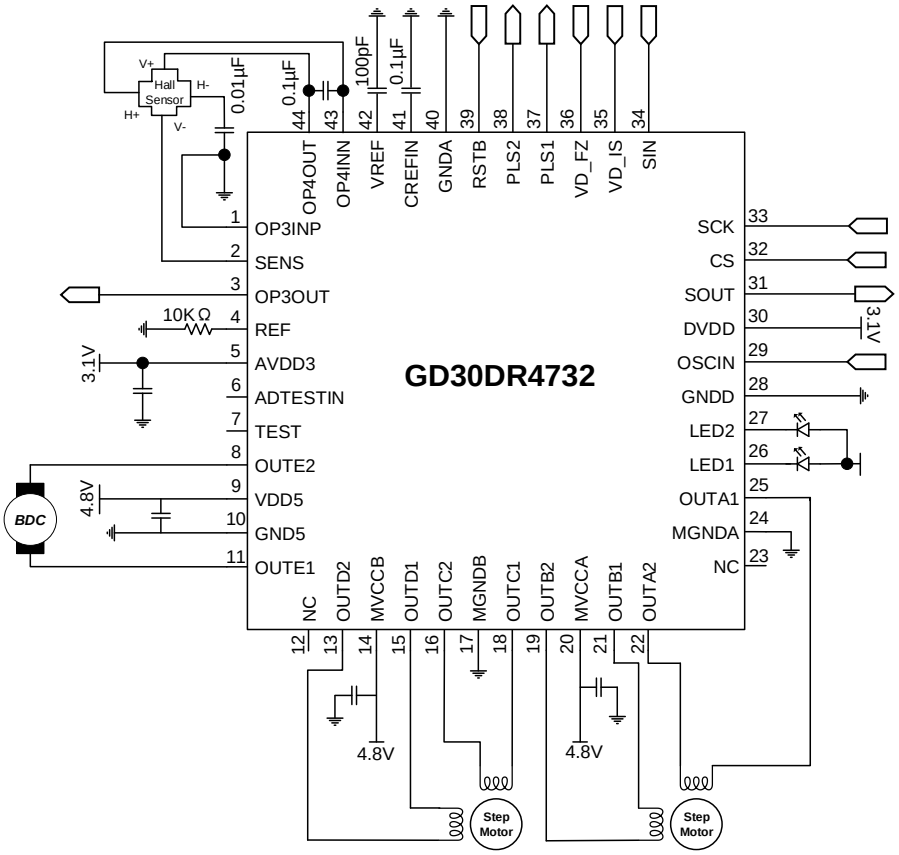

Figure 7. Schematic of GD30DR4732 Application

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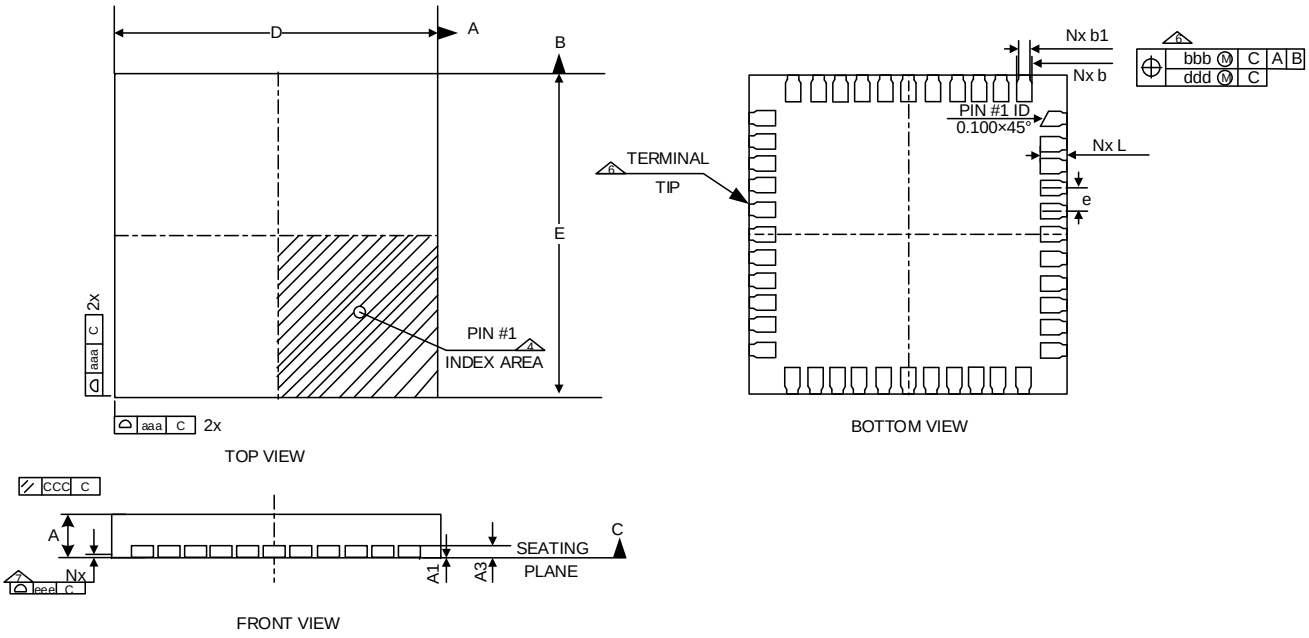
8 Package Information

QFN44 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *QFN44 dimensions(mm)*.

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Table 1. QFN44 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.60	0.65	0.70
A1	-0.01		0.00
A3		0.200 Ref	
b	0.11	0.16	0.21
b1	0.05	0.10	0.15
D	6.00 BSC		
E	6.00 BSC		
e	0.400 BSC		
L	0.50	0.60	0.70
aaa	0.05		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	44		
ND	11		
NE	11		

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9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR4732YUTR-K	QFN44	Green	Tape & Reel	4000	−40°C to +85°C

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10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023

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